AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An error rate determining method ~~for determining~~ which determines an error rate of a semiconductor memory device ~~implementing~~ which implements detection ~~and correction~~ of an error existing in a plurality of pieces of data stored in said semiconductor memory device by using said pieces of data and inspection bits provided for said pieces of data, said error rate determining method comprising ~~the steps of~~:

cumulatively adding a first predetermined value to a total value in the event of detecting a ~~detected~~ first detection signal indicating non-existence of an error in said pieces of data;

subtracting a second predetermined value greater than said first predetermined value from said total value in the event of detecting a ~~detected~~ second detection signal indicating existence of an error in said pieces of data; and

determining said error rate based on ~~the basis of a value of~~ said total value.

2. (Currently Amended) An error rate determining method according to claim 1, ~~whereby~~ wherein said pieces of data and said inspection bits are read ~~out~~ from a memory circuit.

Claims 3-13 (Cancelled)

14. (New) An error rate determining method for a semiconductor memory circuit device having a primary memory circuit and a secondary memory circuit, wherein said primary memory circuit comprises dynamic memory cells, said error rate determining method comprising:

performing a first operation in which when an information sustaining mode is set, a plurality of pieces of data are read from said primary memory circuit to generate inspection bits, and in which the generated inspection bits are stored in said secondary memory circuit;

performing, in a fixed cycle, a second operation in which said pieces of data are read from said primary memory circuit and said inspection bits are read from

said secondary memory circuit to detect whether an error exists in said pieces of data;

adding a first predetermined value to a total value when an error is not detected in said second operation;

subtracting a second predetermined value greater than said first predetermined value from said total value when an error is detected in said second operation; and

adjusting said fixed cycle according to said total value to set an error rate.

15. (New) An error rate determining method according to Claim 14, wherein said fixed cycle is a refresh cycle for said dynamic memory cells.